National Semiconductor

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DS99R421
5-43 MHz FPD-Link LVDS (3 Data + 1 Clock) to Single Embedded Clock DC-Balanced LVDS Converter

General Description

The DS99R421 converts a FPD-Link input with 4 non-DC Balanced LVDS (3 LVDS Data + LVDS Clock) plus 3 oversampled low speed control bits into a single LVDS DC-balanced serial stream with embedded clock information. This single serial stream simplifies transferring the 24-bit bus over a single differential pair of PCB traces and cable by eliminating the skew problems between the 3 parallel LVDS data inputs and LVDS clock paths. It saves system cost by narrowing 4 LVDS pairs to 1 LVDS pair that in turn reduce PCB layers, cable width, connector size, and pins.

The DS99R421 incorporates a single serialized LVDS signal on the high-speed I/O. Embedded clock LVDS provides a low power and low noise environment for reliably transferring data over a serial transmission path. By optimizing the converter output edge rate for the operating frequency range EMI is further reduced.

In addition the device features pre-emphasis to boost signals over longer distances using lossy cables. Internal DC balanced encoding is used to support AC-Coupled interconnects.

Features

- 5 MHz–43 MHz embedded clock & DC-Balanced data transmission (21 total LVDS data bits plus 3 low speed LVCMOS data bits)
- User adjustable pre-emphasis driving ability through external resistor on LVDS outputs and capable to drive up to 10 meters shielded twisted-pair cable
- Supports AC-coupling data transmission
- 100Ω Integrated termination resistor at LVDS input
- Power-down control
- Available @SPEED BIST to DS90UR124 to validate link integrity
- All LVCMOS inputs & control pins have internal pulldown
- Schmitt trigger inputs on OS[2:0] to minimize metastable conditions.
- Outputs Tri-Stated through DEN
- On-chip filters for PLLs
- Power supply range 3.3V ± 10%
- Automotive temperature range –40°C to +105°C
- Greater than 8kV ESD Tolerance
- Meets ISO 10605 ESD and AEC-Q100 compliance

Block Diagram

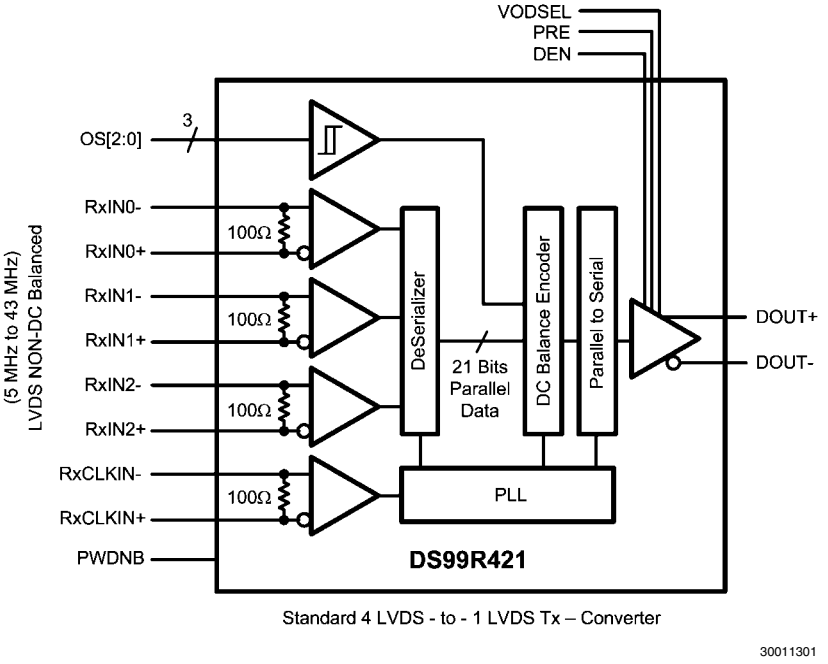


FIGURE 1. Block Diagram

Application Overview

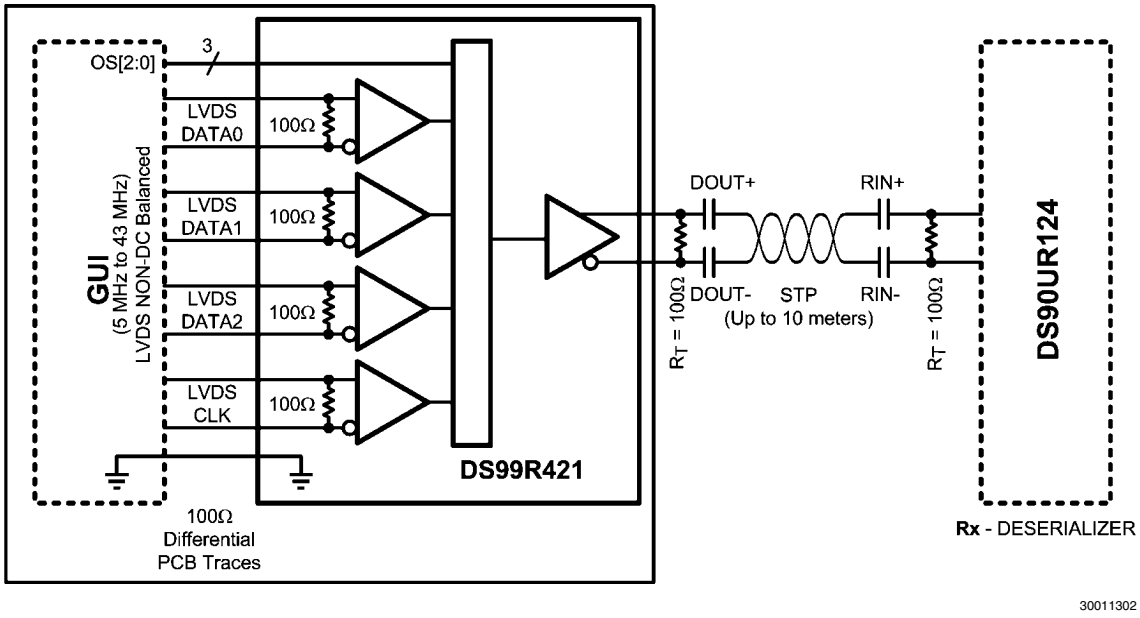


FIGURE 2. Typical Application Diagram

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.3V to +4V
LVCMOS Input Voltage	−0.3V to (V_{DD} +0.3V)
LVCMOS Output Voltage	−0.3V to (V_{DD} +0.3V)
LVDS Receiver Input Voltage	−0.3V to +3.9V
LVDS Driver Output Voltage	−0.3V to +3.9V
LVDS Output Short Circuit Duration	10 ms
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	+260°C
Maximum Package Power Dissipation Capacity	
Package De-rating: DS99R421 − 36L LLP	$1/\theta_{JA}$ °C/W above +25°C
θ_{JA}	37.6 (4L*); 83.7 (2L*)°C/W
θ_{JC}	3.1 (2/4L*) °C/W
	**JEDEC*
ESD Rating (HBM)	≥±8 kV
ESD Rating (ISO10605)	DS99R421 meets ISO10605
R_D = 2 kΩ, C_S = 150/330 pF	
Contact Discharge DOUT±	±10 kV
Air Discharge DOUT±	±25 kV

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DD})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+105	°C
Input Clock Rate RxCLKIN±	5		43	MHz
Supply Noise (V_{DDp-p})			±100	mV_{P-P}
Receiver Input Range	0		V_{DD}	V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
LVCMOS & SCHMITT-TRIGGER INPUT DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage		PWDNB, DEN, VODSEL, BISTEN	2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.9	−1.5	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V		−10		+10	µA
V_{TH}+	High Level Input Voltage		OS[2:0] (Schmitt-triggered Inputs)	2.0			V
V_{TH}−	High Level Input Voltage					0.8	V
V_H	Hysteresis Voltage	V_{TH}+ − V_{TH}−		200	400	600	mV
LVDS DC SPECIFICATIONS							
V_{TH}	Differential Threshold High Voltage	V_{CM} = 1.2V	LVDS differential Inputs: RxIN0±, RxIN1±, RxIN2±, RxCLKIN±			+100	mV
V_{TL}	Differential Threshold Low Voltage			−100			mV
$\|V_{ID}\|$	Differential Input Voltage Swing			100		600	mV
V_{CM}	Common Mode Voltage			0.525	1.2	V_{DD}− (V_{ID}/2)	mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{DD} = 3.6V		−10		+10	µA
		V_{IN} = 0V, V_{DD} = 3.6V		-10		+10	µA

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
V_{OD}	Output Differential Voltage *(Figure 10)*	R_T = 100Ω VODSEL = L	LVDS differential Outputs: DOUT±	380	500	630	mV
		R_T = 100Ω VODSEL = H		650	900	1150	mV
ΔV_{OD}	Output Differential Voltage Unbalance	R_T = 100Ω			10	50	mV
V_{OS}	Output Voltage Offset	R_T = 100Ω PRE = H (off)		1.0	1.2	1.5	V
ΔV_{OS}	Output Voltage Offset Difference	R_T = 100Ω PRE = H (off)			5	50	mV
I_{OS}	Output Short Circuit Current	DOUT± = 0V VODSEL = L PRE = H (off)		−2		−8	mA
		DOUT± = 0V VODSEL = H PRE = H (off)		−7		−13	mA
I_{OZ}	TRI-STATE Output Current	PWDNB = 0V, DOUT± = 0V OR V_{DD} *(inputs not toggling)*		−10	±1	+10	µA
R_T	Internal Input Termination Resistance		**RxIN:** across RxIN(2:0)+ & RxIN (2:0)−, and across RxCLKIN+ & RxCLKIN−	90	105	130	Ω
CONVERTER SUPPLY CURRENT							
I_{DD}	Total Supply Current (includes load current)	R_T = 100Ω CHECKERBOARD pattern PRE = 6 KΩ *(Figure 3)*	f = 43 MHz		95	130	mA
I_{DDTZ}	Supply Current Power-down	PWDNB = 0V *(inputs not toggling)*			2	50	µA

Receiver Input Timing Requirements

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{RCIH}	Receiver Clock Input High Time	Referenced to rising edge of RxCLKIN	0.35T	0.57T		ns
t_{RCIL}	Receiver Clock Input Low Time	Referenced to rising edge of RxCLKIN		0.43T	0.65T	ns

Receiver Input Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
RITOL-L	Receiver Input Tolerance Left *(Figures 7, 8)* (Notes 8, 10)		5 MHz–43 MHz			0.3	UI
RITOL-R	Receiver Input Tolerance Right *(Figures 7, 8)* (Notes 8, 10)		5 MHz–43 MHz			0.3	UI
UI	Unit Interval (Note 8)		5 MHz–43 MHz		1/7th of RxCLKIN		ns

Input Timing Requirements for OS[2:0]

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
F_{OS}[2:0]	Maximum Frequency Limitation of OS[2:0]		OS[2:0]			$F_{RxCLKIN}$ / 5	MHz

Input to Output Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
RCTCD	RxCLK IN to DOUT Delay *(Figure 5)*, (Note 9)		5 MHz–43 MHz	4T + 1.0	4T + 5.0	4T + 10.0	ns
PDD	Power Down Delay		5 MHz–43 MHz			1	µs

Serializer Output Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LLHT}	LVDS Low-to-High Transition Time	R_T = 100Ω, C_L = 10 pF to GND *(Figure 4)*		0.3	0.5	ns
t_{LHLT}	LVDS High-to-Low Transition Time			0.3	0.5	ns
t_{PLT}	PLL Lock Time	5 MHz–43 MHz			10	ms
TxOUT_E_O	TxOUT_Eye_Opening (Notes 8, 11) *(Figure 9)*	5 MHz–43 MHz *(respect to ideal)*	0.78			UI
UI	Unit Interval (Note 8)	5 MHz–43 MHz		1/28th of DOUT		ns

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: Typical values represent most likely parametric norms at 3.3V, Ta = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 4: Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD}, ΔV_{OD}, V_{TH} and V_{TL} which are differential voltages.

Note 5: Specification is guaranteed by characterization and is not tested in production.

Note 6: Specification is guaranteed by design and is not tested in production.

Note 7: Total Interconnect Jitter Budget (t_{JIT}) specifies the allowable jitter added by the interconnect assuming both transmitter and receiver are SerDes circuits.

Note 8: UI – Unit Interval, equivalent to one ideal serialized data bit width. The UI scales with frequency.

For the input, it is 1/7th the input clock period. Example 43 MHz = 23.26 ns. 1/7th of this is 3.32 ns. This is 1 UI of the input at 43 MHz.

For the output, it is 1/28th of the input clock period. Example 43 MHz = 23.26 ns. 1/28th of this is 831 ps. This is 1 UI of the output at 43 MHz.

Note 9: A Clock Unit Symbol (T) is defined as 1/ (Line rate of RxCLKIN).

Note 10: Receiver Input Tolerance is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window – RSPos). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter.

Note 11: TxOUT_E_O is affected by pre-emphasis value.

AC Timing Diagrams and Test Circuits

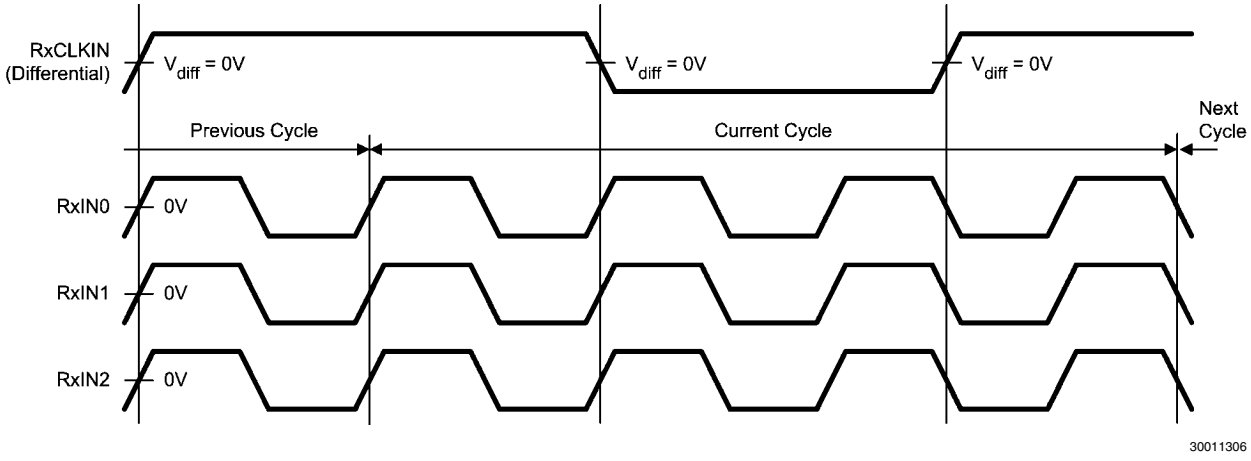


FIGURE 3. LVDS Input Checkerboard Pattern

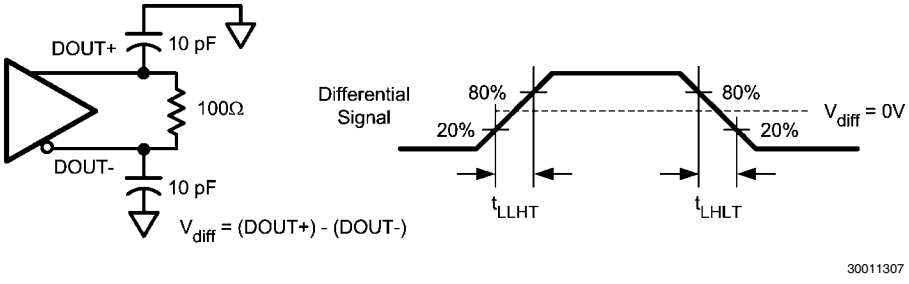


FIGURE 4. Serializer LVDS Output Load and Transition Times

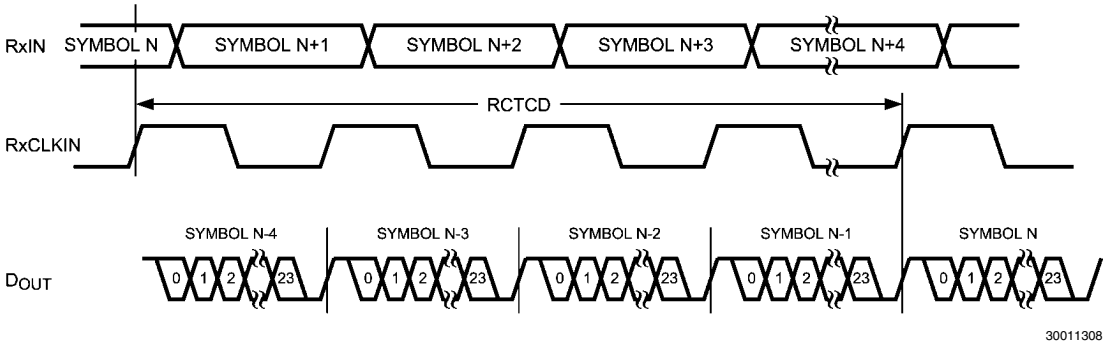


FIGURE 5. RxIN to DOUT Delay – RCTCD

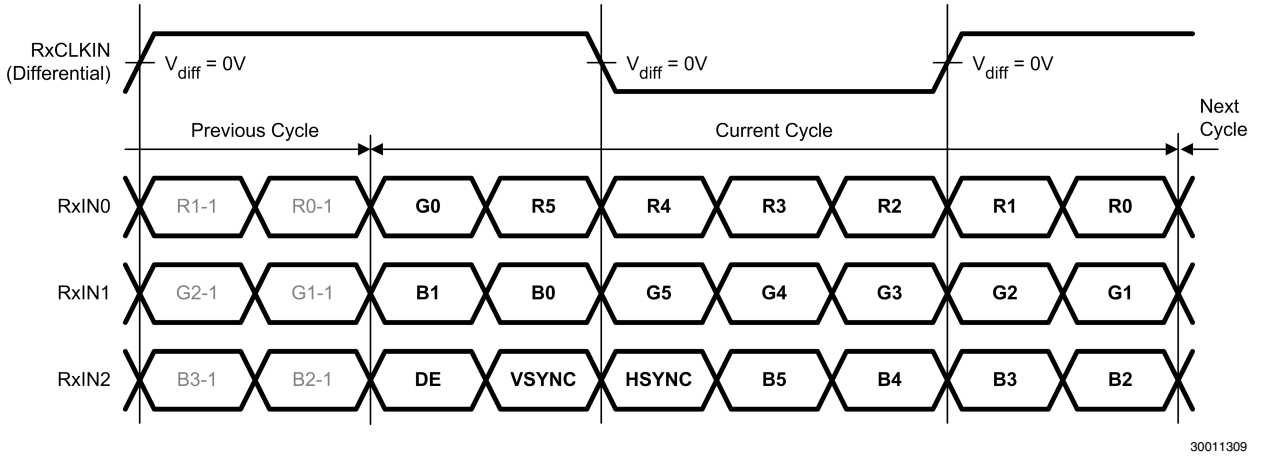


FIGURE 6. Receiver LVDS Input Mapping

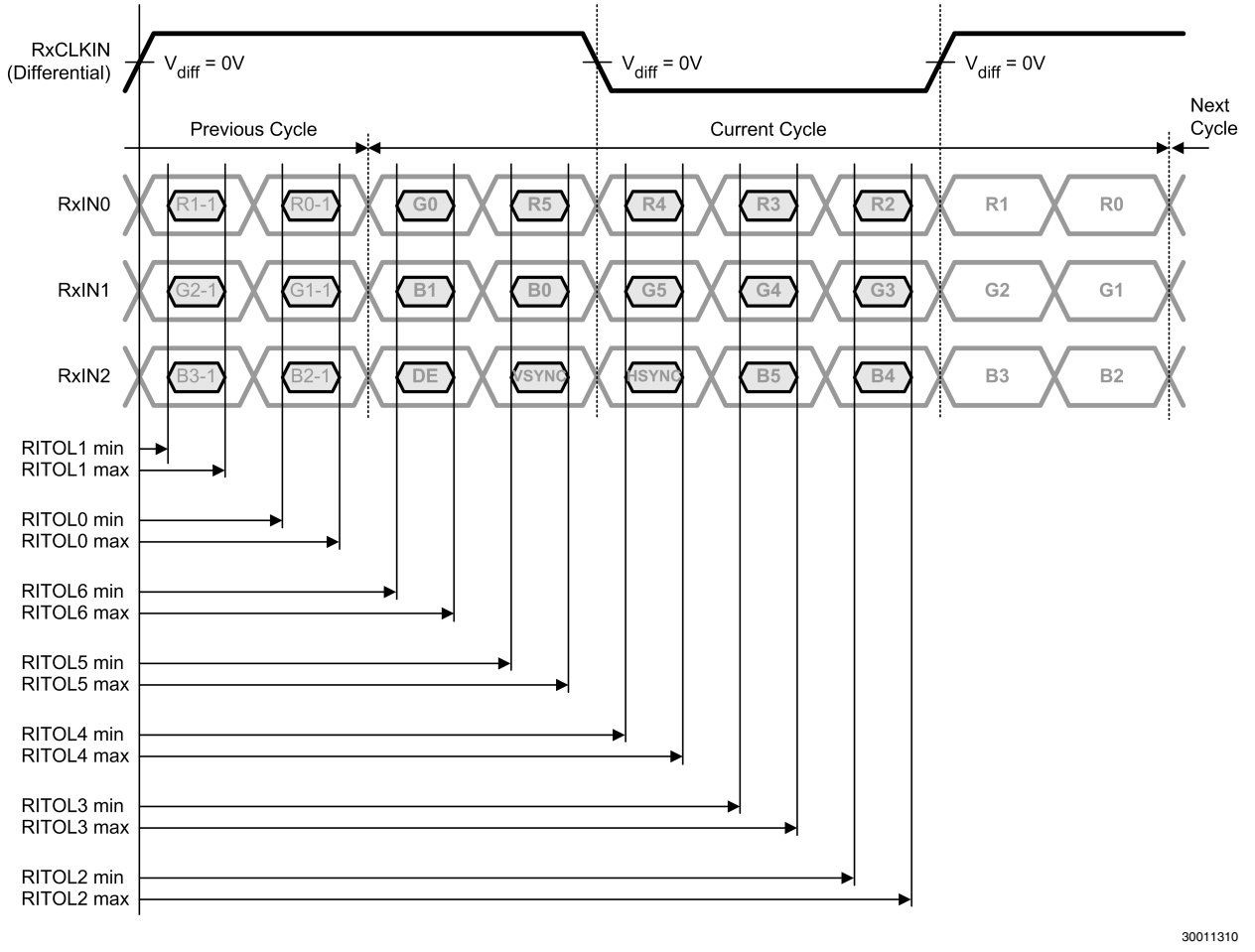


FIGURE 7. Receiver RITOL Min and Max

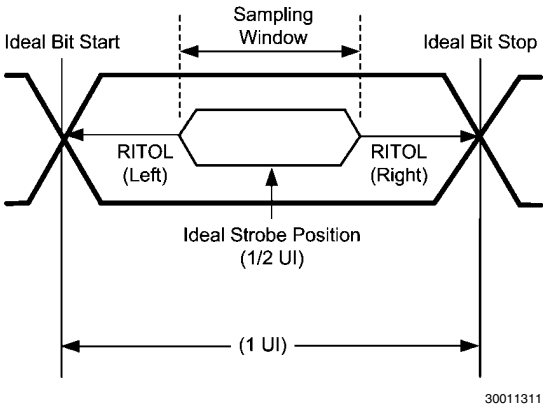


FIGURE 8. Receiver RITOL Left and Right

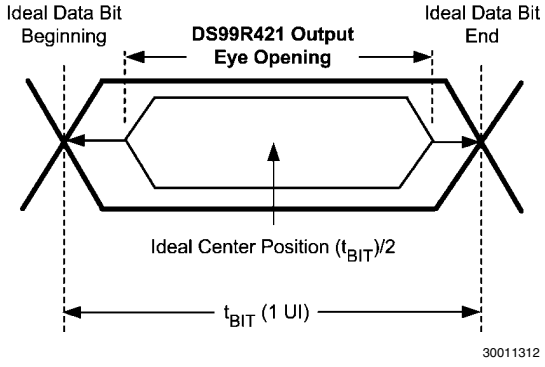


FIGURE 9. Serializer Output Eye Opening

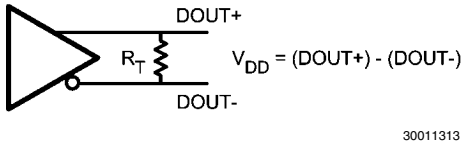


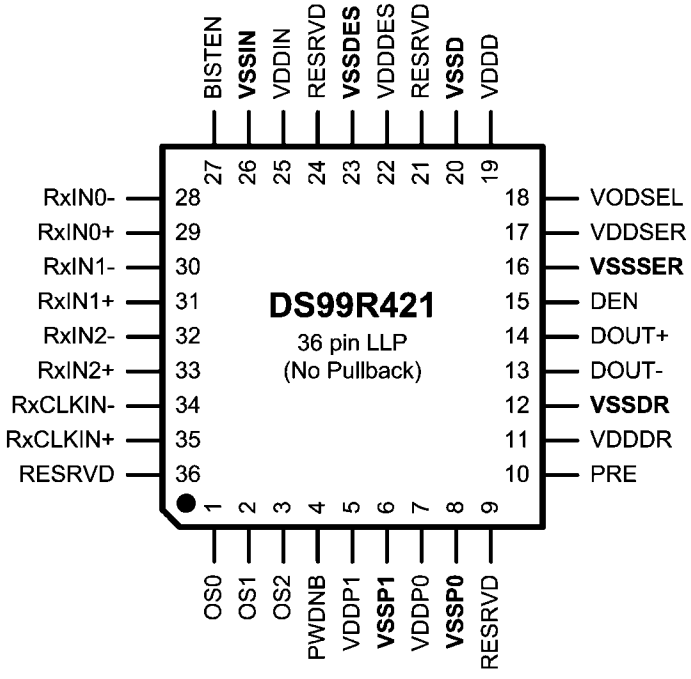
FIGURE 10. Serializer V_{OD} Diagram

Pin Descriptions

Pin #	Pin Name	I/O/PWR	Description
FPD-LINK LVDS RECEIVER INPUT PINS			
28, 30, 32	RxIN[2:0]–	LVDS_I	LVDS Receiver inverted Data Inputs (–)
29, 31, 33	RxIN[2:0]+	LVDS_I	LVDS Receiver true Data Inputs (+)
34	RxCLKIN–	LVDS_I	LVDS Receiver inverted reference Clock Inputs. Used to strobe data at the RxIN inputs and to drive the receiver PLL
35	RxCLKIN+	LVDS_I	LVDS Receiver true reference Clock Inputs. Used to strobe data at the RxIN inputs and to drive the receiver PLL
OVER SAMPLED INPUT PINS			
3-1	OS[2:0]	LVCMOS_I	Over Sampled Receiver Data Inputs with Schmitt trigger
CONTROL AND CONFIGURATION PINS			
4	PWDNB	LVCMOS_I	Power Down Bar PWDNB = H; Device is Enabled and ON PWDNB = L; Device is in power down mode (Sleep), LVDS Driver D_{OUT} (+/-) Outputs are in TRI-STATE stand-by mode, PLL is shutdown to minimize power consumption.
15	DEN	LVCMOS_I	Data Enable DEN = H; LVDS Driver Outputs are Enabled (ON). DEN = L; LVDS Driver Outputs are Disabled (OFF), Serializer LVDS Driver D_{OUT} (+/-) Outputs are in TRI-STATE, PLL still operational and locked to TCLK.
10	PRE	LVCMOS_I	Pre-emphasis Level Select PRE = NC (No Connect); Pre-emphasis is Disabled (OFF). Pre-emphasis is active when input is tied to VSS through external resistor R_{PRE}. Resistor value determines pre-emphasis level. Recommended value $R_{PRE} \geq 6\ k\Omega$; $I_{max} = [48 / R_{PRE}]$, $R_{PREmin} = 6\ k\Omega$ See Applications Information section for more details.
18	VODSEL	LVCMOS_I	VOD Level Select VODSEL = L; LVDS Driver Output is ±500 mV ($R_T = 100\Omega$) VODSEL = H; LVDS Driver Output is ±900 mV ($R_T = 100\Omega$) For normal applications, set this pin LOW. For long cable applications where a larger VOD is required, set this pin HIGH. See Applications Information section for more details.
36, 24, 21, 9	RESRVD	LVCMOS_I/O	Reserved. This pin **MUST** be tied LOW.
BIST MODE PINS			
27	BISTEN	LVCMOS_I	Control Pin for BIST Mode Enable (ACTIVE H) BISTEN = L; Default at Low, Normal Mode BISTEN = H; BIST mode active Note: Sequence order for proper function of BIST mode: 1) DS99R421 BISTEN = H. 2) DS99R421 PLL must be locked (10 ms). 3) DS90UR124 PLL must be locked. 4) Select BISTM error reporting mode on DS90UR124. 5) DS90UR124 switch BISTEN from L to H.
LVDS SERIALIZER OUTPUT PINS			
14	DOUT+	LVDS_O	Serializer LVDS True **(+)** Output. This output is intended to be loaded with a 100Ω load to the D_{OUT+} pin. The interconnect should be AC Coupled to this pin with a 100 nF capacitor.
13	DOUT–	LVDS_O	Serializer LVDS Inverted **(-)** Output This output is intended to be loaded with a 100Ω load to the D_{OUT-} pin. The interconnect should be AC Coupled to this pin with a 100 nF capacitor.
POWER / GROUND PINS			
5	V_{DD}P1	V_{DD}	Analog Power supply, PLL POWER
6	V_{SS}P1	GND	Analog Ground, PLL GROUND

Pin #	Pin Name	I/O/PWR	Description
7	V_{DD}P0	V_{DD}	Analog Power supply, VCO POWER
8	V_{SS}P0	GND	Analog Ground, VCO GROUND
11	V_{DD}DR	V_{DD}	Analog Power supply, LVDS OUTPUT POWER
12	V_{SS}DR	GND	Analog Ground, LVDS OUTPUT GROUND
17	V_{DD}SER	V_{DD}	Digital Power supply, SERIALIZER POWER
16	V_{SS}SER	GND	Digital Ground, SERIALIZER GROUND
19	V_{DD}D	V_{DD}	Digital Power supply, LOGIC POWER
20	V_{SS}D	GND	Digital Ground, LOGIC GROUND
22	V_{DD}DES	V_{DD}	Digital Power supply, RECEIVER POWER
23	V_{SS}DES	GND	Digital Ground, RECEIVER GROUND
25	V_{DD}IN	V_{DD}	Analog Power supply, LVDS INPUT POWER
26	V_{SS}IN	GND	Analog Ground, LVDS INPUT GROUND

Pin Diagram — DS99R421



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TOP VIEW

Functional Description

The DS99R421 is a Video Interface converter. It converts an FPD-Link interface (3 LVDS data channels + 1 LVDS Clock, e.g. DS90C365A or equivalent) plus up to three (3) LVCMOS additional signals into a single high-speed LVDS serial Interface (see *Figure 11*).

The 21 bits of data from the FPD-Link Interface are serialized along with the 3 additional over-sampled bits (OS[2:0]) into a randomized, scrambled and DC Balanced data stream to support AC coupling and to enhance the signal eye opening. Four (4) additional overhead bits are sent per clock which provides the embedded clock and serial link control information. The embedded clock LVDS serial stream has an effective data throughput of 120 Mbps (5MHz X 24) to 1.03 Gbps (43MHz X 24). The DS99R421 Line Driver is designed to transmit data up to 10 meters over shielded twisted pair (STP) at signaling rates up to 1.2Gbps (43MHz X 28).

The DS90UR124 receiver converts the embedded clock LVDS stream back into a 24-bit wide LVCMOS parallel bus and the recovered low-speed clock.

Note: The *DS90C124* is not compatible with the DS99R421.

LINK START UP

The start up of the DS99R421 involves only one PLL Lock time. The FPD-Link Receiver side must lock to its incoming LVDS RxCLKIN. The Serializer side then extracts its reference clock from the incoming LVDS clock. At the far end of the link, the Deserializer (DS90UR124) also needs to detect the LVDS signals and lock to the incoming serial stream, drives the LOCK pin HIGH, before outputting valid data. Note that when using a Bus Converter (FPD-Link to Serial) additional time is required in the start up to account for the additional PLLs in the path.

TYPICAL START UP SEQUENCE

1. FPD-Link Stream is applied to the DS99R421 inputs.
2. With power applied and the DS99R421 enabled, it will lock to the incoming FPD-Link clock. Until the DS99R421 is ready, it will hold its outputs in TRI-STATE. Once the locking is complete, valid serial payloads are sent across the link to the DES (DS90UR124).
3. With power applied and the device enabled, the DS90UR124 will lock to the incoming serial stream. Until the DS90UR124 is locked, outputs are in TRI-STATE and its LOCK output pin is held Low. After Lock, the DS90UR124 outputs are active and LOCK is HIGH.

DATA TRANSFER

After the link start up, the DS99R421 provides a streaming video interface. For each Pixel Clock (PCLK) received from the FPD-Link Interface 21 bits of information are recovered along with the PCLK. The 21 bits of information include the 18-bits of RGB information and the three video control signals (HS, VS and DE). The over-sample control bits are also sampled in this PCLK domain and appended to the 21 bits of information for a 24-bit total payload. The Serializer side now takes this data and performs four operations to it. First the data is randomized, second the data is scrambled, third the data is balanced, and finally the serial link control and clock embedding is done. The Serializer transmits 28 bits of information per payload to the Deserializer per PCLK. See DS90UR241 datasheet for additional information on the Serializer's description and operation.

The chipset supports PCLK frequency ranges of 5 MHz to 43 MHz. At the 43MHz PCLK rate, 28 bits are sent across the serial link at 1.2Gbps. The link is very efficient, sending 25 bits of information (18 RGB, 3 control, 3 over-sample control, and PCLK) with 28 serial bits. This yields 89% efficiency.

DS99R421 LINE DRIVER

The DS99R421 output (DOUT±) is used to drive a point-to-point connection as shown in *Figure 12*. The Line driver transmits data when the data enable pin (DEN) is HIGH, the power down bar (PWDNB) is HIGH, and the device is locked to the incoming FPD-Link stream. If the DEN is set LOW, the device remains locked, but the driver outputs are placed in TRI-STATE. This maybe used to provide a fast start up since a lock time is not required.

PRE-EMPHASIS

The DS99R421 features a Pre-Emphasis function used to compensate for extra long or lossy transmission media. Cable drive is enhanced with a user selectable Pre-Emphasis feature that provides additional output current during transitions to counteract cable loading effects. The transmission distance will be limited by the loss characteristics and quality of the media.

To enable the Pre-Emphasis function, the "PRE" pin requires one external resistor (Rpre) to Vss in order to set the additional current level. Options include:

Normal Output (no pre-emphasis) – Leave the PRE pin open

Enhanced Output (pre-emphasis enabled) – connect a resistor on the PRE pin to Vss. Values of the PRE Resistor should be between 6K Ohm and 100M Ohm. Values less than 6K Ohm should not be used. The amount of Pre-Emphasis for a given media will depend on the transmission distance and Fmax of the application. In general, too much Pre-Emphasis can cause over or undershoot at the receiver input pins. This can result in excessive noise, crosstalk, reduced Fmax, and increased power dissipation. For shorter cables or distances, Pre-Emphasis is typically not be required. Signal quality measurements should be made at the end of the application cable to confirm the proper amount of Pre-Emphasis for the specific application.

The Pre-Emphasis circuit increases the drive current to I = 48 / (Rpre). For example if Rpre = 15K Ohm, then the Pre-Emphasis current is increased by an additional 3.2 mA.

The duration of the current is controlled to precisely one bit by another circuit. If more than one bit value is repeated in the next cycle(s), the next bit(s) is "de-emphasized"; Pre-Emphasis is turned off (back to the normal output current level, hence output level is also reduced). This is done to reduce power, and to reduce ISI (Inter-Symbol Interference).

VOD SELECT

The Serializer Line Driver Differential Output Voltage (VOD) magnitude is selectable. Two levels are provided and are determined by the state of the VODSEL pin. When this pin is LOW, normal output levels are obtained. For most application set the VODSEL pin LOW. When this pin is HIGH, the output current is increased to increase the VOD level. Use this setting only for extra long cable or high-loss interconnects.

OVER-SAMPLED BITS – OS[2:0]

Up to three additional signals maybe sent across the serial link per PCLK. The over-sampled bits are restricted to be low speed signals and should be less than 1/5 of the frequency of the PCLK. The DS99R421 OS[2:0] LVCMOS Inputs have wide hysteresis to help prevent glitches. Signals should convey level information only, as pulse width distortion will occur by the over sampling technique and location of the sampling

clock. The three over sampled bits are mapped to DS90UR124 bits as: OS0 = bit 21, OS1 = bit 22, and OS2 = bit 23. If the OS bits are not required, internal pull-down will bias the input to a LOW.

COLOR MAPPING

Color mapping is application specific. It is very important to properly match the Pixel bit to the correct data channel on the DS90UR124 to properly recover the color and control information. See *Figure 11*. In this example, the G0 color bit is placed in the RxIN0 channel and is the first bit. The Serializer in the DS99R421 will place this bit as bit number 6. Thus G0 will be recovered by the DS90UR124 on bit 6. The three over sampled bits are mapped to DS90UR124 bits as: OS0 = bit 21, OS1 = bit 22, and OS2 = bit 23.

POWERDOWN (SLEEP) MODE

The Powerdown state is a low power sleep mode that the DS99R421 and DS90UR124 may use to reduce power when no data is being transferred. The PWDNB on the DS99R421 and RPWDNB on the DS90UR124 are used to set each device into power down mode, which reduces supply current to the µA range. The DS99R421 enters powerdown when the PWDNB pin is driven LOW. In powerdown, the PLL stops and the outputs go into TRI-STATE, disabling load current and reducing current supply. To powerup, the DS99R421, PWDNB must be driven HIGH. When the DS99R421 exits powerdown, its PLL must lock to RxCLKIN before it is ready for the initialization state. The system must then allow time for initialization before data transfer can begin.

SERIAL INTERFACE

The serial link between the DS99R421 and the DS90UR124 is intended for a balanced 100 Ohm interconnect. The link is expected to be terminated at both ends with 100 Ohms and AC coupled.

To establish a source termination and the correct levels, a Driver side termination is required. This is typically located close to the device pins and is 100 Ohm resistor connected across the driver outputs.

The AC coupling capacitors should be place close to the 100 Ohm termination resistor at both ends of the interface. For the high-speed LVDS transmission, small footprint packages should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics. NPO class 1 or X7R class 2 type capacitors are recommended. 50 WVDC should be the minimum used for best system-level ESD performance. The most common used capacitor value for the interface is 100 nF (0.1 uF) capacitor.

The DS90UR124 input stage is designed for AC-coupling by providing a built-in AC bias network which sets the internal V_{CM} to +1.8V. Therefore multiple termination options are possible.

Receiver Termination Option 1

A single 100 Ohm termination resistor is placed across the RIN± pins (see *Figure 12*). This provides the signal termination at the Receiver inputs. Other options may be used to increase noise tolerance.

Receiver Termination Option 2

For additional EMI tolerance, two 50 Ohm resistors may be used in place of the single 100 Ohm resistor. A small capacitor is tied from the center point of the 50 Ohm resistors to ground (see *Figure 14*). This provides a high-frequency low-impedance path for noise suppression. Value is not critical, 4.7nF maybe used with general applications.

Receiver Termination Option 3

For high noise environments an additional voltage divider network may be connected to the center point. This has the advantage of a providing a DC low-impedance path for noise suppression. Use resistor values in the range of 100Ω-1KΩ for the pullup and pulldown. Ratio the resistor values to bias the center point at 1.8V. For example (see *Figure 15*): V_{DD}=3.3V, Rpullup=1KΩ, Rpulldown=1.2KΩ; or Rpullup=100Ω, Rpulldown=120Ω (strongest). The smaller values will consume more bias current, but will provide enhanced noise suppression.

FPD LINK INTERFACE

The FPD-Link Interface supports a 3 Data + Clock (21 bit) interface. The interconnect should employ a 100 Ohm differential pair, as termination is provided internal to the DS99R421. Note that color mapping is extremely important to review. Color placement of the bits on the FPD-Link Interface will determine which outputs they will be recovered on. The DS99R421 is expected to reside on the same board as the FPD-Link Serializer (e.g. DS90C365A or GUI with Integrated FPD-Link Serializer). The DS99R421 supports a limited common mode range of 525mV to (VDD – VID/2). Typically this is wide enough to support short interconnects.

@SPEED-BIST (BUILT IN SELF TEST)

The DS99R421/ DS90UR124 serial link is equipped with a built-in self-test (BIST) capability to support both system manufacturing and field diagnostics.

BIST mode is intended to check the entire high-speed serial link at full link-speed, without the use of specialized and expensive test equipment. This feature provides a simple method for a system host to perform diagnostic testing of both DS99R421 and DS90UR124. The BIST function is easily configured through the 2 control pins (BISTEN and BISTM) on the DS90UR124 and one control pin (BISTEN) of the DS99R421. When the BIST mode is activated, the DS99R421 has the ability to transfer an internally generated PRBS data pattern. This pattern traverses across interconnecting links to the DS90UR124. The DS90UR124 includes an on-chip PRBS pattern verification circuit that checks the data pattern for bit errors and reports any errors on the data output pins on the DS90UR124.

The @SPEED-BIST feature uses 2 control pins (BISTEN and BISTM) on the DS90UR124 Deserializer. The BISTEN and BISTM pins together determine the functions of the BIST mode. The BISTEN signal (HIGH) activates the test feature on the DS90UR124. After the BIST mode is enabled on the DS90UR124, toggle the BISTEN pin HIGH on the DS99R421 for the DS90UR124 Deserializer to start accepting data. An input clock signal (RxCLKIN) for the DS99R421 must also be applied during the entire BIST operation. Data on RxIN[2:0] and OS[2:0] are ignored during operation of the BIST. The BISTM pin on the DS90UR124 selects the error reporting status mode of the BIST function. When BIST is configured in the error status mode (BISTM = LOW), each of the ROUT [23:0] outputs of the DS90UR124 will correspond to bit errors on a cycle-by-cycle basis. The result of bit mismatches are indicated on the respective parallel inputs on the ROUT[23:0] data output pins. In the BIST error count accumulator mode (BISTM = HIGH), an 8-bit counter on ROUT[7:0] is used to represent the number of errors detected (0 to 255 max). The successful completion of the BIST test is reported on the PASS pin on the DS90UR124 Deserializer. The DS90UR124 Deserializer's PLL must first be locked to ensure the PASS status is valid. The PASS status pin will stay LOW and then

transition to HIGH once a BER of $1x10^{-9}$ is achieved across the transmission link.

Applications Information

USING THE DS99R421 AND DS90UR124

The DS99R421 allows a FPD-Link based bus to connect to a single-channel serial LVDS interface in a Display using the latest generation LVDS Deserializer (DS90UR124). This allows for existing hosts with FPD-Link interfaces to be further serialized into a single pair and connect with the current generation Display Deserializer. Systems benefit by the smaller interconnect (reduced pins, less size, lower cost).

DISPLAY APPLICATION

18-bit color depth (RGB666) and up to 1280 X 480 display formats can be supported. In a RGB666 configuration 18 color bits (R[5:0], G [5:0], B[5:0]), Pixel Clock (PCLK) and three control bits (VS, HS and DE) along with three low speed spare bits OS[2:0] are supported across the serial link with PCLK rates from 5 to 43MHz.

TYPICAL APPLICATION CONNECTION

Figure 13 shows a typical connection to the DS99R421.

The 4 pairs of FPD-Link LVDS interface are the input interface along with the optional over-sampled control signals. Termination of the LVDS signals is provided internally by the DS99R421 device.

The single channel LVDS serial output requires an external termination and also AC coupling capacitors.

Configuration pins for the typical application are shown:

DEN – tie HIGH if unused.

PWDNB – Sleep / Enable Control Input – Connect to host or tie HIGH

BISTEN – tie LOW if not used, or connect or host

VODSEL – tie LOW for normal VOD magnitude (application dependant)

PRE – Leave open if not required (have a R pad option on PCB)

RESRVD – tie LOW (4 pins)

There are 4 power rails for the device. These may be bussed together on a common 3.3V plane. At a minimum, four 0.1uF capacitors should be used for local bypassing.

With the above configuration a FPD-Link interface along with three additional low-speed signals are converted to a single serial LVDS channel.

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the LVDS SERDES devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with vias on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz range. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Termination of the LVDS interconnect is required. For point-to-point applications, termination should be located at both ends of the devices. Nominal value is 100 Ohms to match the line's differential impedance. Place the resistor as close to the transmitter DOUT± outputs and receiver RIN± inputs as possible to minimize the resulting stub between the termination resistor and device.

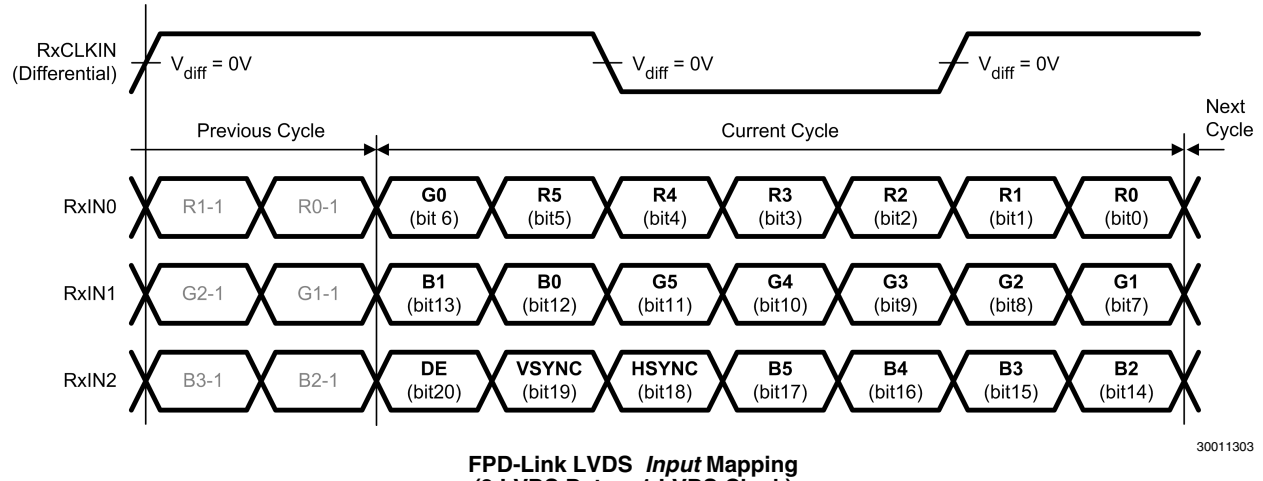
LVDS INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

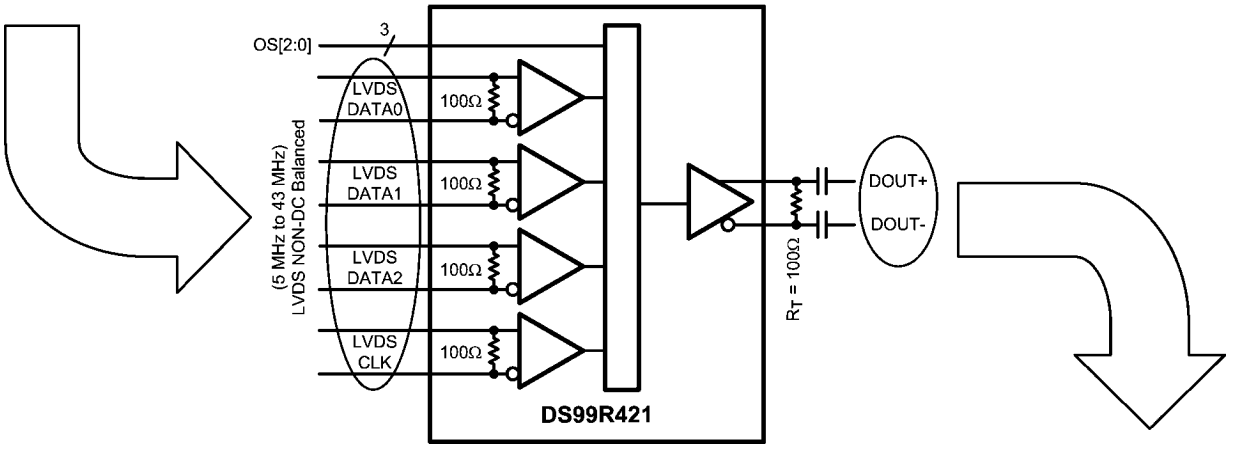
- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in separation
  —S = space between the pair
  —2S = space between pairs
  —3S = space to LVCMOS signal
- Minimize the number of vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

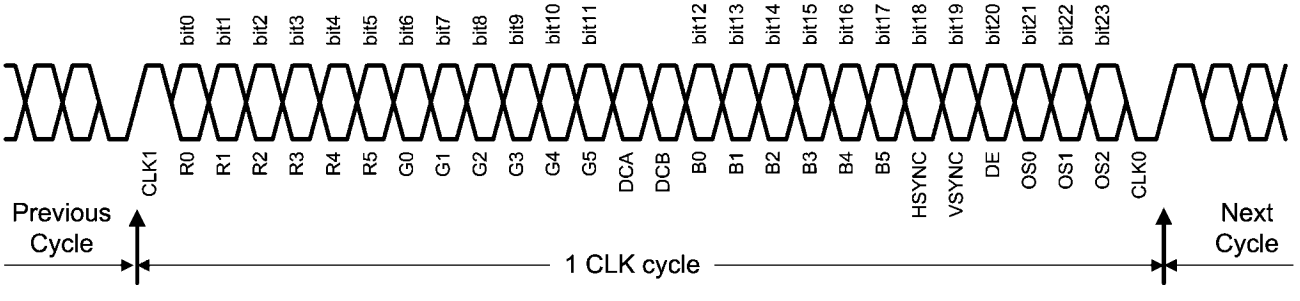
Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the National web site at: **www.national.com/lvds**

Functional Overview



FPD-Link LVDS *Input* Mapping
(3 LVDS Data + 1 LVDS Clock)





* Note: bits [0-23] are not physically located in positions shown above since bits [0-23] are scrambled and DC Balanced

Single Serialized LVDS Bitstream*

FIGURE 11. LVDS Data Mapping Diagram

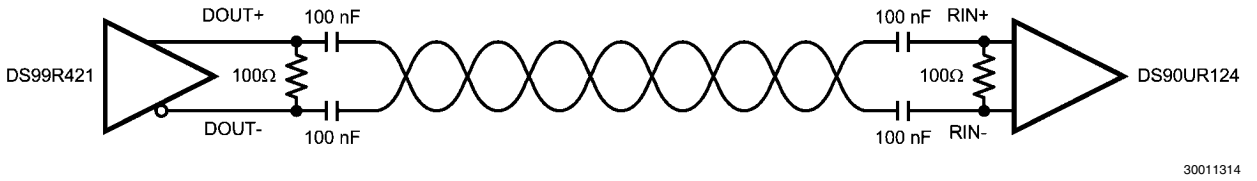


FIGURE 12. AC Coupled Application

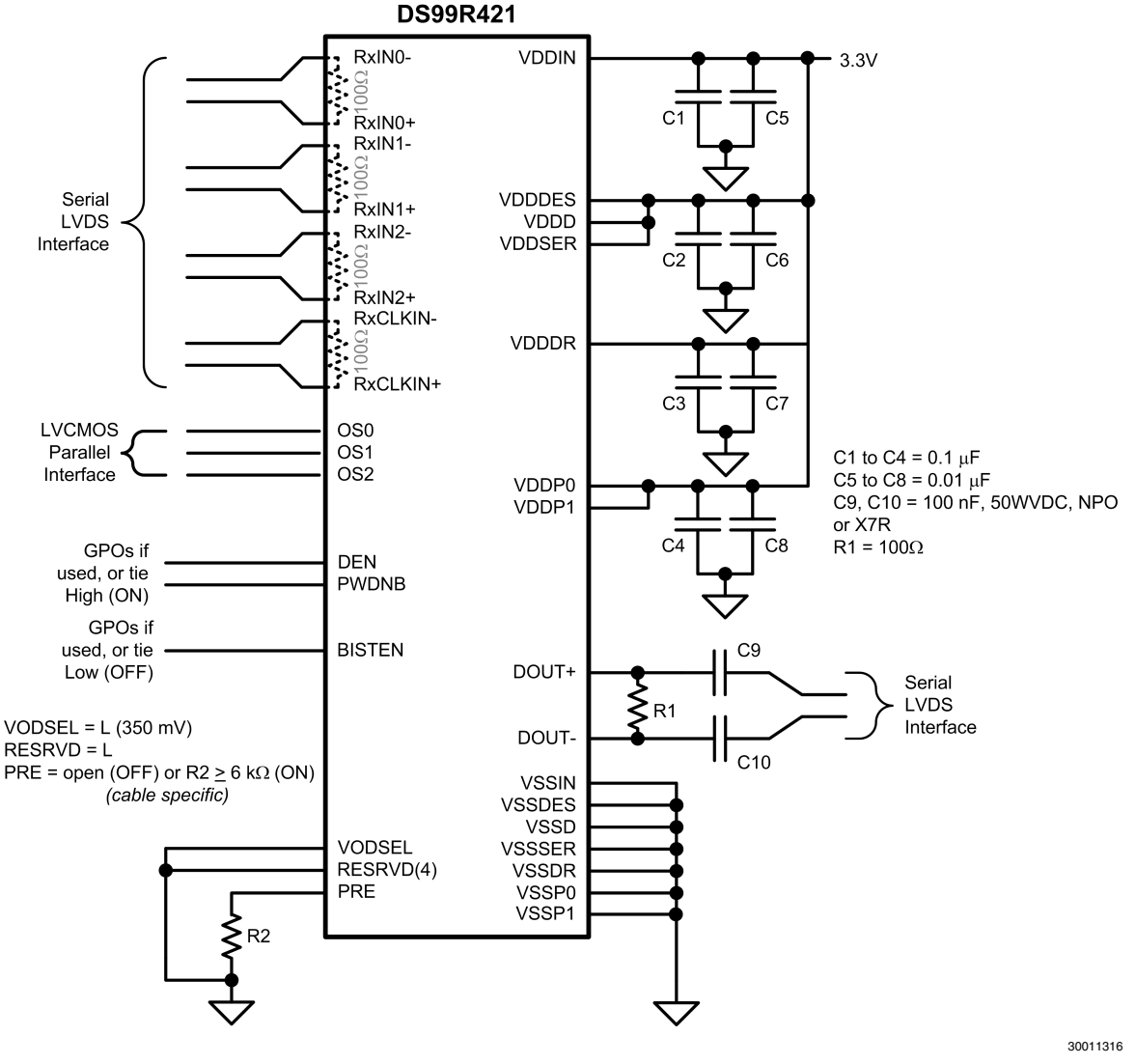


FIGURE 13. DS99R421 Typical Application Connection

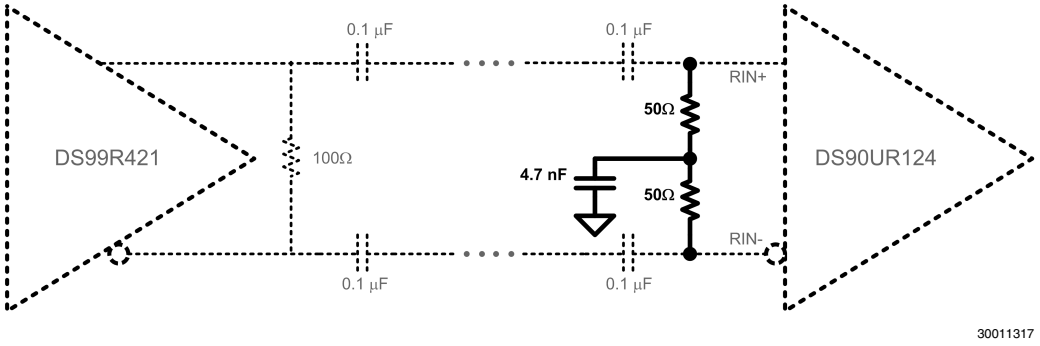


FIGURE 14. Receiver Termination Option 2

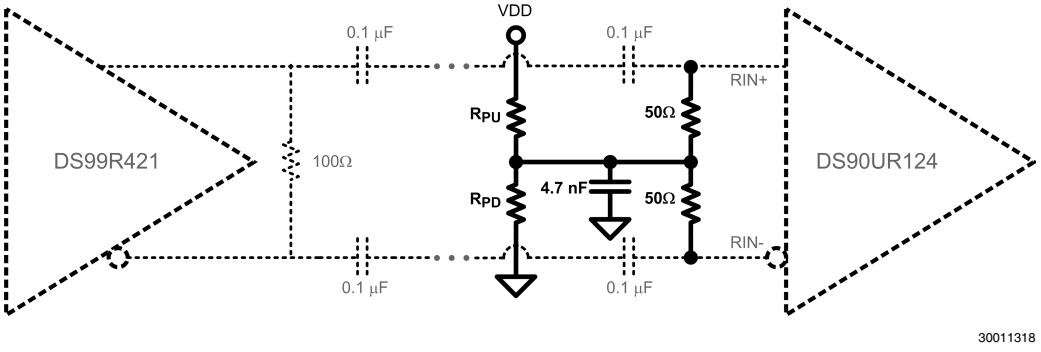
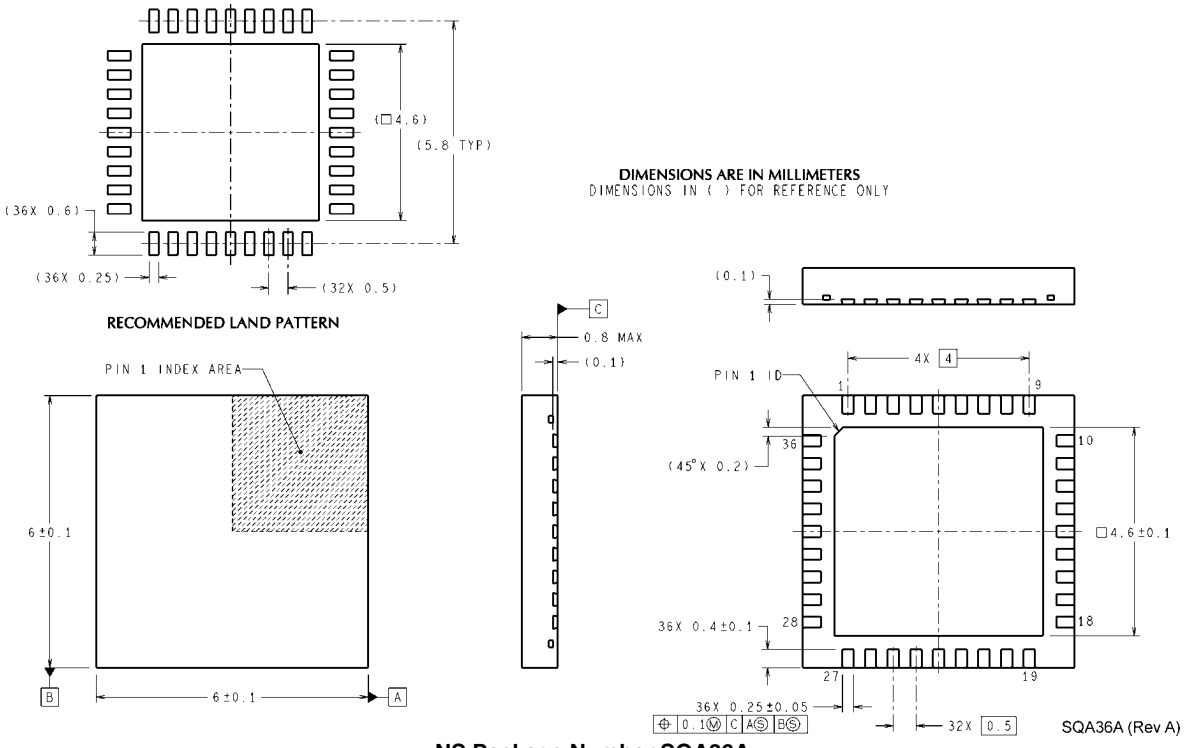


FIGURE 15. Receiver Termination Option 3

Physical Dimensions inches (millimeters) unless otherwise noted



NS Package Number SQA36A

Ordering Information

NSID	Package Type	Package ID
DS99R421QSQ	36-Lead LLP, 6.0 X 6.0 X 0.8 mm, 0.5 mm pitch	SQA36A
DS99R421QSQX	36-Lead LLP, 6.0 X 6.0 X 0.8 mm, 0.5 mm pitch, 2500 std reel	SQA36A
DS99R421ISQ	36-Lead LLP, 6.0 X 6.0 X 0.8 mm, 0.5 mm pitch	SQA36A
DS99R421ISQX	36-Lead LLP, 6.0 X 6.0 X 0.8 mm, 0.5 mm pitch, 2500 std reel	SQA36A

Notes

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Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
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Switching Regulators	www.national.com/switchers		
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